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ABSTRACT

A novel mask layer is used in the dual damascene construction of an interconnect structure of an integrated circuit device. The interconnect structure has a low-k dielectric material. The mask layer has a passivation film deposited on the low-k dielectric  
5 material. The mask layer has a passivation film deposited on the low-k dielectric material, a barrier film is deposited over the passivation film and a metallic film is deposited over the barrier film. The metallic film increases the overall etch selectivity of the mask layer to assure a faithful transfer of via and trench features to the low-k dielectric material during the etching steps of the dual damascene process.

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